CY7C1316CV18
CY7C1916CV18
CY7C1318CV18
CY7C1320CV18

PRELIMINARY

18-Mbit DDR-II SRAM 2-Word Burst Architecture

Features

- **18-Mbit density (2M x 8, 2M x 9, 1M x 18, 512K x 36)**
- **300-MHz clock for high bandwidth**
- **2-Word burst for reducing address bus frequency**
- **Double Data Rate (DDR) interfaces (data transferred at 600 MHz) @ 300 MHz**
- **Two input clocks (K and $\overline{K}$) for precise DDR timing**
  - **— SRAM uses rising edges only**
- **Two input clocks for output data (C and $\overline{C}$) to minimize clock-skew and flight-time mismatches**
- **Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high-speed systems**
- **Synchronous internally self-timed writes**
- **DDR-II operates with 1.5 cycle read latency when the DLL is enabled**
- **Operates like a DDR-I device with 1 cycle read latency in DLL off mode**
- **1.8V core power supply with HSTL inputs and outputs**
- **Variable drive HSTL output buffers**
- **Expanded HSTL output voltage (1.4V–V_{DD})**
- **Available in 165-ball FBGA package (13 x 15 x 1.4 mm)**
- **Offered in both lead-free and non lead-free packages**
- **JTAG 1149.1-compatible test access port**
- **Delay Lock Loop (DLL) for accurate data placement**

Configurations

CY7C1316CV18 – 2M x 8

CY7C1916CV18 – 2M x 9

CY7C1318CV18 – 1M x 18

CY7C1320CV18 – 512K x 36

Functional Description

The CY7C1316CV18, CY7C1916CV18, CY7C1318CV18 and CY7C1320CV18 are 1.8V Synchronous Pipelined SRAM equipped with DDR-II architecture. The DDR-II consists of an SRAM core with advanced synchronous peripheral circuitry and a 1-bit burst counter. Addresses for Read and Write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of C and $\overline{C}$ if provided, or on the rising edge of K and $\overline{K}$ if C/$\overline{C}$ are not provided. Each address location is associated with two 8-bit words in the case of CY7C1316CV18 and two 9-bit words in the case of CY7C1916CV18 that burst sequentially into or out of the device. The burst counter always starts with a "0" internally in the case of CY7C1316CV18 and CY7C1916CV18. On CY7C1318CV18 and CY7C1320CV18, the burst counter takes in the least significant bit of the external address and bursts two 18-bit words in the case of CY7C1318CV18 and two 36-bit words in the case of CY7C1320CV18 sequentially into or out of the device.

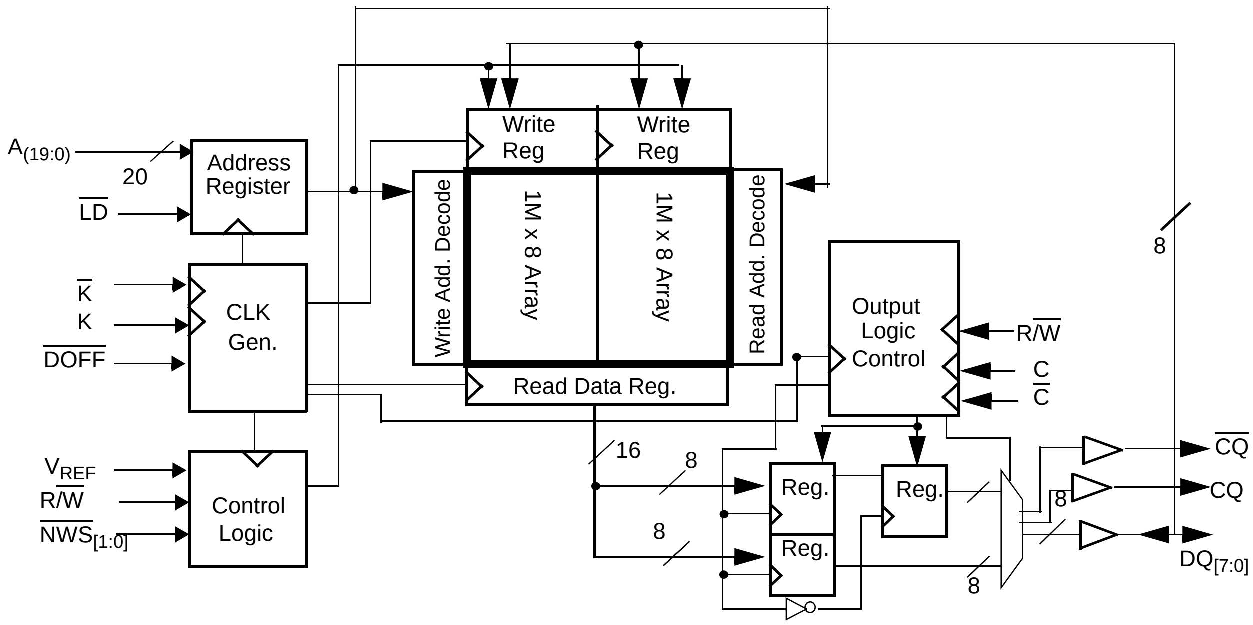
Asynchronous inputs include output impedance matching input (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need for separately capturing data from each individual DDR SRAM in the system design. Output data clocks (C/$\overline{C}$) enable maximum system clocking and data synchronization flexibility.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the C or $\overline{C}$ (or K or $\overline{K}$ in a single clock domain) input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

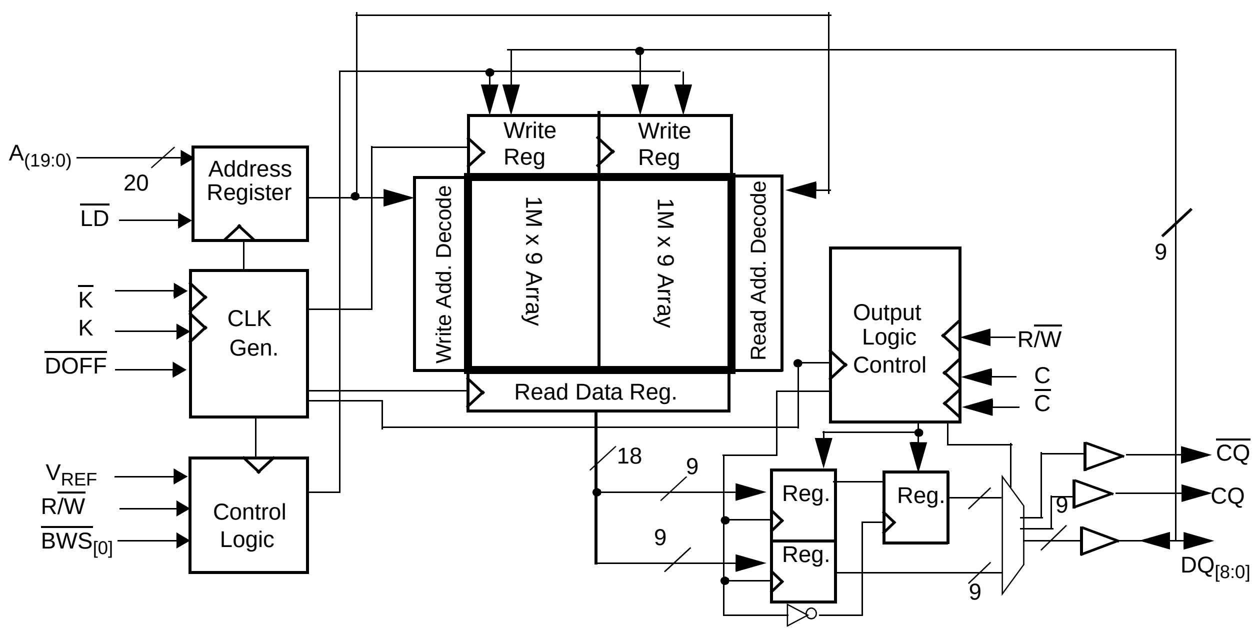
Selection Guide

	300 MHz	278 MHz	250 MHz	200 MHz	167 MHz	Unit
Maximum Operating Frequency	300	278	250	200	167	MHz
Maximum Operating Current	600	580	550	500	450	mA

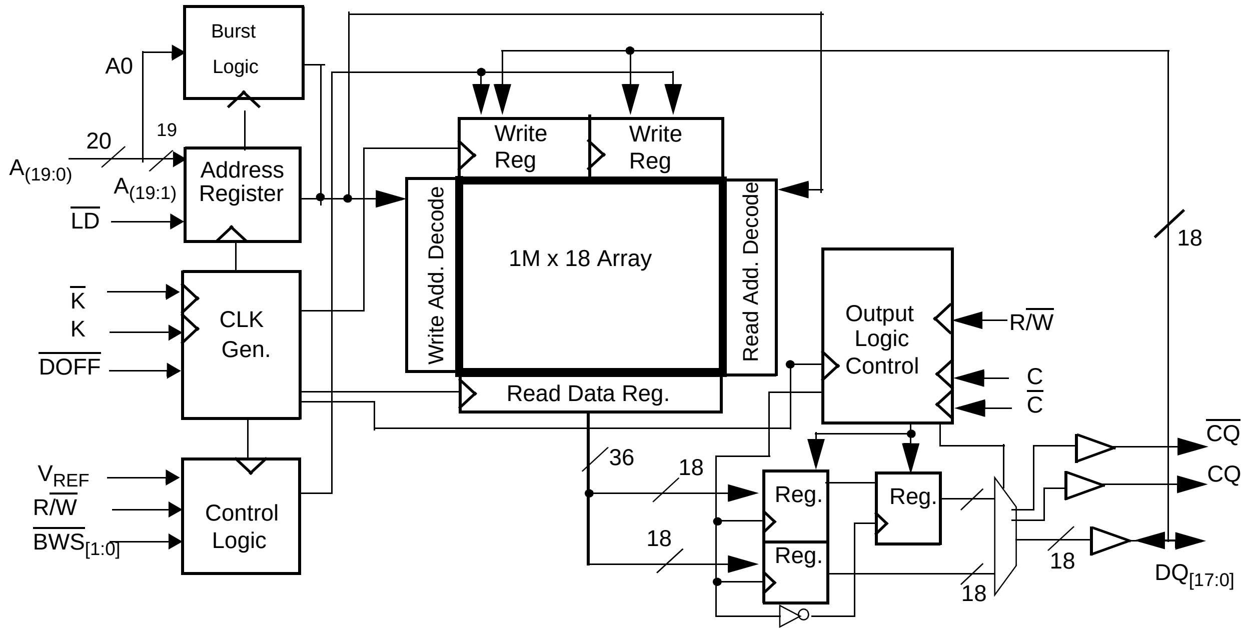
Logic Block Diagram (CY7C1316CV18)



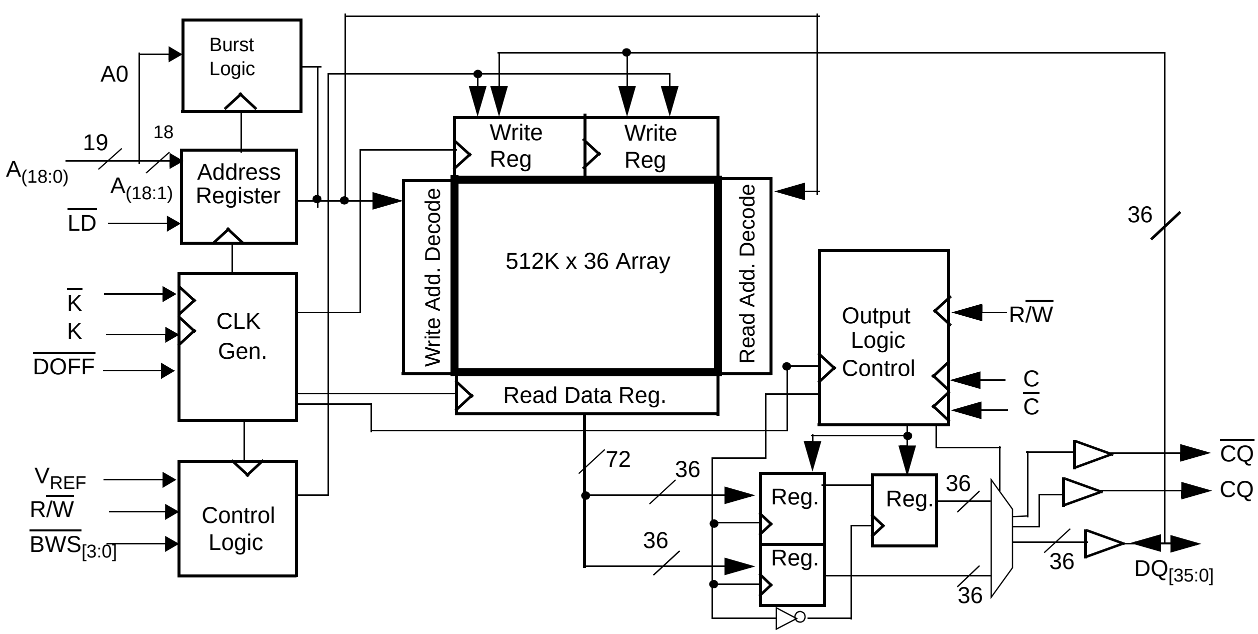
Logic Block Diagram (CY7C1916CV18)



Logic Block Diagram (CY7C1318CV18)



Logic Block Diagram (CY7C1320CV18)



Pin Configurations

165-ball FBGA (13 x 15 x 1.4 mm) Pinout

CY7C1316CV18 (2M x 8)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	$R/\overline{W}$	$\overline{NWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	NC/36M	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{NWS_0}$	A	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	A	A	C	A	A	NC	NC	NC
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

CY7C1916CV18 (2M x 9)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	$R/\overline{W}$	NC	$\overline{K}$	NC/144M	$\overline{LD}$	A	NC/36M	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	A	A	C	A	A	NC	NC	DQ8
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Pin Configurations (continued)

165-ball FBGA (13 x 15 x 1.4 mm) Pinout

CY7C1318CV18 (1M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	$R/\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	NC/36M	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	A0	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	C	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

CY7C1320CV18 (512K x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	NC/36M	$R/\overline{W}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{LD}$	A	NC/72M	CQ
B	NC	DQ27	DQ18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	A	A0	A	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	A	A	A	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	A	A	C	A	A	NC	DQ9	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Pin Definitions

Pin Name	I/O	Pin Description
$DQ_{[x:0]}$	Input/Output-Synchronous	**Data Input/Output signals**. Inputs are sampled on the rising edge of K and $\overline{K}$ clocks during valid Write operations. These pins drive out the requested data during a Read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during Read operations or K and $\overline{K}$ when in single clock mode. When read access is deselected, $Q_{[x:0]}$ are automatically tri-stated. CY7C1316CV18 – $DQ_{[7:0]}$ CY7C1916CV18 – $DQ_{[8:0]}$ CY7C1318CV18 – $DQ_{[17:0]}$ CY7C1320CV18 – $DQ_{[35:0]}$
$\overline{LD}$	Input-Synchronous	**Synchronous Load**. This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and Read/Write direction. All transactions operate on a burst of 2 data.
$\overline{NWS}_0$, $\overline{NWS}_1$	Input-Synchronous	**Nibble Write Select 0, 1 – active LOW (CY7C1316CV18 only)**. Sampled on the rising edge of the K and $\overline{K}$ clocks during Write operations. Used to select which nibble is written into the device during the current portion of the Write operations. Nibbles not written remain unaltered. $\overline{NWS}_0$ controls $D_{[3:0]}$ and $\overline{NWS}_1$ controls $D_{[7:4]}$. All the Nibble Write Selects are sampled on the same edge as the data. Deselecting a Nibble Write Select will cause the corresponding nibble of data to be ignored and not written into the device.
$\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$, $\overline{BWS}_3$	Input-Synchronous	**Byte Write Select 0, 1, 2, and 3 – active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during Write operations. Used to select which byte is written into the device during the current portion of the Write operations. Bytes not written remain unaltered. CY7C1916CV18 – $\overline{BWS}_0$ controls $D_{[8:0]}$ CY7C1318CV18 – $\overline{BWS}_0$ controls $D_{[8:0]}$ and $\overline{BWS}_1$ controls $D_{[17:9]}$. CY7C1320CV18 – $\overline{BWS}_0$ controls $D_{[8:0]}$, $\overline{BWS}_1$ controls $D_{[17:9]}$, $\overline{BWS}_2$ controls $D_{[26:18]}$ and $\overline{BWS}_3$ controls $D_{[35:27]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select will cause the corresponding byte of data to be ignored and not written into the device.
A, A0	Input-Synchronous	**Address Inputs**. These address inputs are multiplexed for both Read and Write operations. Internally, the device is organized as 2M x 8 (2 arrays each of 1M x 8) for CY7C1316CV18 and 2M x 9 (2 arrays each of 1M x 9) for CY7C1916CV18, a single 1M x 18 array for CY7C1318CV18, and a single array of 512K x 36 for CY7C1320CV18. CY7C1316CV18 – Since the least significant bit of the address internally is a “0,” only 20 external address inputs are needed to access the entire memory array. CY7C1916CV18 – Since the least significant bit of the address internally is a “0,” only 20 external address inputs are needed to access the entire memory array. CY7C1318CV18 – A0 is the input to the burst counter. These are incremented in a linear fashion internally. 20 address inputs are needed to access the entire memory array. CY7C1320CV18 – A0 is the input to the burst counter. These are incremented in a linear fashion internally. 19 address inputs are needed to access the entire memory array. All the address inputs are ignored when the appropriate port is deselected.
R/$\overline{W}$	Input-Synchronous	**Synchronous Read/Write Input**. When $\overline{LD}$ is LOW, this input designates the access type (Read when R/$\overline{W}$ is HIGH, Write when R/$\overline{W}$ is LOW) for loaded address. R/$\overline{W}$ must meet the set-up and hold times around edge of K.
C	Input-Clock	**Positive Input Clock for Output Data.** C is used in conjunction with $\overline{C}$ to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
$\overline{C}$	Input-Clock	**Negative Input Clock for Output Data**. $\overline{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
K	Input-Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input-Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous data being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.

Pin Definitions (continued)

Pin Name	I/O	Pin Description
CQ	Output-Clock	**CQ is referenced with respect to C**. This is a free running clock and is synchronized to the input clock for output data (C) of the DDR-II. In the single clock mode, CQ is generated with respect to K. The timings for the echo clocks are shown in the AC Timing table.
$\overline{CQ}$	Output-Clock	**$\overline{CQ}$ is referenced with respect to $\overline{C}$**. This is a free running clock and is synchronized to the input clock for output data ($\overline{C}$) of the DDR-II. In the single clock mode, $\overline{CQ}$ is generated with respect to $\overline{K}$. The timings for the echo clocks are shown in the AC Timing table.
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**DLL Turn Off - Active LOW**. Connecting this pin to ground will turn off the DLL inside the device. The timings in the DLL turned off operation will be different from those listed in this data sheet. For normal operation, this pin can be connected to a pull-up through a 10-Kohm or less pull-up resistor. The device will behave in DDR-I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with DDR-I timing.
TDO	Output	**TDO for JTAG**.
TCK	Input	**TCK pin for JTAG**.
TDI	Input	**TDI pin for JTAG**.
TMS	Input	**TMS pin for JTAG**.
NC	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/36M	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/72M	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/144M	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/288M	N/A	**Not connected to the die**. Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs and Outputs as well as AC measurement points.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the device**.
V_{DDQ}	Power Supply	**Power supply inputs for the outputs of the device**.

Functional Overview

The CY7C1316CV18, CY7C1916CV18, CY7C1318CV18, and CY7C1320CV18 are synchronous pipelined Burst SRAMs equipped with a DDR interface which operates with a read latency of one and half cycles when $\overline{DOFF}$ pin is tied HIGH. When $\overline{DOFF}$ pin is set LOW or connected to V_{SS} the device will behave in DDR-I mode with a read latency of one clock cycle.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and $\overline{K}$) and all output timing is referenced to the rising edge of the output clocks (C/$\overline{C}$ or K/$\overline{K}$ when in single clock mode).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the output clocks (C/$\overline{C}$ or K/$\overline{K}$ when in single-clock mode).

All synchronous control (R/$\overline{W}$, $\overline{LD}$, $\overline{BWS}_{[0:X]}$) inputs pass through input registers controlled by the rising edge of the input clock (K).

CY7C1318CV18 is described in the following sections. The same basic descriptions apply to CY7C1316CV18, CY7C1916CV18, and CY7C1320CV18.

Read Operations

The CY7C1318CV18 is organized internally as a single array of 1M x 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting R/$\overline{W}$ HIGH and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to Address inputs is stored in the Read address register and the least significant bit of the address is presented to the burst counter. The burst counter increments the address in a linear fashion. Following the next K clock rise the corresponding 18-bit word of data from this address location is driven onto the $Q_{[17:0]}$ using $\overline{C}$ as the output timing reference. On the subsequent rising edge of C the next 18-bit data word from the address location generated by the burst counter is driven onto the $Q_{[17:0]}$. The requested data will be valid 0.45 ns from the rising

edge of the output clock (C or $\overline{C}$, or K and $\overline{K}$ when in single clock mode, 200-MHz and 250-MHz device). In order to maintain the internal logic, each read access must be allowed to complete. Read accesses can be initiated on every rising edge of the positive input clock (K).

When Read access is deselected, the CY7C1318CV18 will first complete the pending Read transactions. Synchronous internal circuitry will automatically tri-state the outputs following the next rising edge of the positive output clock (C). This will allow for a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting R/$\overline{W}$ LOW and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to Address inputs is stored in the Write address register and the least significant bit of the address is presented to the burst counter. The burst counter increments the address in a linear fashion. On the following K clock rise the data presented to $D_{[17:0]}$ is latched and stored into the 18-bit Write Data register provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the Negative Input Clock ($\overline{K}$) the information presented to $D_{[17:0]}$ is also stored into the Write Data register provided $\overline{BWS}_{[1:0]}$ are both asserted active. The 36 bits of data are then written into the memory array at the specified location. Write accesses can be initiated on every rising edge of the positive input clock (K). Doing so will pipeline the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When Write access is deselected, the device will ignore all inputs after the pending Write operations have been completed.

Byte Write Operations

Byte Write operations are supported by the CY7C1318CV18. A Write operation is initiated as described in the Write Operations section above. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$ which are sampled with each set of 18-bit data word. Asserting the appropriate Byte Write Select input during the data portion of a Write will allow the data being presented to be latched and written into the device. Deasserting the Byte Write Select input during the data portion of a write will allow the data stored in the device for that byte to remain unaltered. This feature can be used to simplify Read/Modify/Write operations to a Byte Write operation.

Single Clock Mode

The CY7C1318CV18 can be used with a single clock that controls both the input and output registers. In this mode the device will recognize only a single pair of input clocks (K and $\overline{K}$) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/$\overline{K}$ and C/$\overline{C}$ clocks. All timing parameters remain the same in this mode. To use this mode of operation, the user must tie C and $\overline{C}$ HIGH at power-on. This function is a strap option and not alterable during device operation.

DDR Operation

The CY7C1318CV18 enables high-performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation. The CY7C1318CV18 requires a single No Operation (NOP) cycle when transitioning from a Read to a Write cycle. At higher frequencies, some applications may require a second NOP cycle to avoid contention.

If a Read occurs after a Write cycle, address and data for the Write are stored in registers. The Write information must be stored because the SRAM cannot perform the last word Write to the array without conflicting with the Read. The data stays in this register until the next Write cycle occurs. On the first Write cycle after the Read(s), the stored data from the earlier Write will be written into the SRAM array. This is called a Posted Write.

If a Read is performed on the same address on which a Write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

Depth Expansion

Depth expansion requires replicating the $\overline{LD}$ control signal for each bank. All other control signals can be common between banks as appropriate.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM, The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175Ω and 350Ω, with V_{DDQ} = 1.5V. The output impedance is adjusted every 1024 cycles upon power-up to account for drifts in supply voltage and temperature.

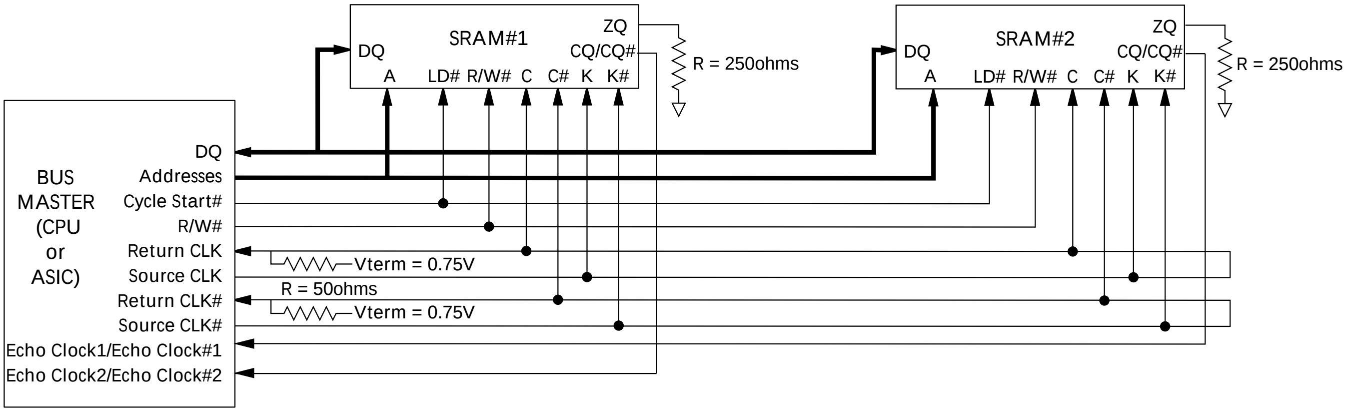
Echo Clocks

Echo clocks are provided on the DDR-II to simplify data capture on high-speed systems. Two echo clocks are generated by the DDR-II. CQ is referenced with respect to C and $\overline{CQ}$ is referenced with respect to $\overline{C}$. These are free-running clocks and are synchronized to the output clock of the DDR-II. In the single clock mode, CQ is generated with respect to K and $\overline{CQ}$ is generated with respect to $\overline{K}$. The timings for the echo clocks are shown in the AC Timing table.

DLL

These chips utilize a Delay Lock Loop (DLL) that is designed to function between 80 MHz and the specified maximum clock frequency. During power-up, when the DOFF is tied HIGH, the DLL gets locked after 1024 cycles of stable clock. The DLL can also be reset by slowing or stopping the input clock K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary for the DLL to be specifically reset in order to lock the DLL to the desired frequency. The DLL will automatically lock 1024 clock cycles after a stable clock is presented. The DLL may be disabled by applying ground to the DOFF pin. When the DLL is turned off, the device will behave in DDR-I mode (with one cycle latency and a longer access time). For information refer to the application note “DLL Considerations in QDRII™/DDRII”.

Application Example[1]



Truth Table[2, 3, 4, 5, 6, 7]

Operation	K	$\overline{LD}$	R/$\overline{W}$	DQ	DQ
Write Cycle: Load address; wait one cycle; input write data on consecutive K and $\overline{K}$ rising edges.	L-H	L	L	D(A1) at K(t + 1) ↑	D(A2) at $\overline{K}$(t + 1) ↑
Read Cycle: Load address; wait one and a half cycle; read data on consecutive $\overline{C}$ and C rising edges.	L-H	L	H	Q(A1) at $\overline{C}$(t + 1)↑	Q(A2) at C(t + 2) ↑
NOP: No Operation	L-H	H	X	High-Z	High-Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State

Burst Address Table

(CY7C1318CV18, CY7C1320CV18)

First Address (External)	Second Address (Internal)
X..X0	X..X1
X..X1	X..X0

Notes:
1. The above application shows two DDR-II used.
2. X = “Don’t Care,” H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
3. Device will power-up deselected and the outputs in a tri-state condition.
4. On CY7C1318CV18 and CY7C1320CV18, “A1” represents address location latched by the devices when transaction was initiated and A2 represents the addresses sequence in the burst. On CY7C1316CV18, “A1” represents A + ‘0’ and A2 represents A + ‘1’.
5. “t” represents the cycle at which a Read/Write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the “t” clock cycle.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on C and $\overline{C}$ rising edges, except when in single clock mode.
7. It is recommended that K = $\overline{K}$ and C = $\overline{C}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

Write Cycle Descriptions (CY7C1316CV18 and CY7C1318CV18) [2, 8]

$\overline{BWS_0}$,$\overline{NWS_0}$	$\overline{BWS_1}$,$\overline{NWS_1}$	K	$\overline{K}$	Comments
L	L	L-H	–	During the Data portion of a Write sequence: CY7C1316CV18 – both nibbles ($D_{[7:0]}$) are written into the device, CY7C1318CV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L-H	During the Data portion of a Write sequence: CY7C1316CV18 – both nibbles ($D_{[7:0]}$) are written into the device, CY7C1318CV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L-H	–	During the Data portion of a Write sequence: CY7C1316CV18 – only the lower nibble ($D_{[3:0]}$) is written into the device. $D_{[7:4]}$ will remain unaltered, CY7C1318CV18 – only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
L	H	–	L-H	During the Data portion of a Write sequence: CY7C1316CV18 – only the lower nibble ($D_{[3:0]}$) is written into the device. $D_{[7:4]}$ will remain unaltered, CY7C1318CV18 – only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
H	L	L-H	–	During the Data portion of a Write sequence: CY7C1316CV18 – only the upper nibble ($D_{[7:4]}$) is written into the device. $D_{[3:0]}$ will remain unaltered, CY7C1318CV18 – only the upper byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ will remain unaltered.
H	L	–	L-H	During the Data portion of a Write sequence: CY7C1316CV18 – only the upper nibble ($D_{[7:4]}$) is written into the device. $D_{[3:0]}$ will remain unaltered, CY7C1318CV18 – only the upper byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ will remain unaltered.
H	H	L-H	–	No data is written into the devices during this portion of a Write operation.
H	H	–	L-H	No data is written into the devices during this portion of a Write operation.

Note:

8. Assumes a Write cycle was initiated per the Write Port Cycle Description Truth Table. $\overline{NWS_0}$, $\overline{NWS_1}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a Write cycle, as long as the set-up and hold requirements are achieved.

Write Cycle Descriptions (CY7C1320CV18) [2, 8]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_2}$	K	$\overline{K}$	Comments
L	L	L	L	L-H	–	During the Data portion of a Write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L-H	During the Data portion of a Write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L-H	–	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ will remain unaltered.
L	H	H	H	–	L-H	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ will remain unaltered.
H	L	H	H	L-H	–	During the Data portion of a Write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ will remain unaltered.
H	L	H	H	–	L-H	During the Data portion of a Write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ will remain unaltered.
H	H	L	H	L-H	–	During the Data portion of a Write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ will remain unaltered.
H	H	L	H	–	L-H	During the Data portion of a Write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ will remain unaltered.
H	H	H	L	L-H		During the Data portion of a Write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ will remain unaltered.
H	H	H	L	–	L-H	During the Data portion of a Write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ will remain unaltered.
H	H	H	H	L-H	–	No data is written into the device during this portion of a Write operation.
H	H	H	H	–	L-H	No data is written into the device during this portion of a Write operation.

Write Cycle Descriptions[2, 8] (CY7C1916CV18)

$\overline{BWS_0}$	K	$\overline{K}$	Comments
L	L-H	–	During the Data portion of a Write sequence, the single byte ($D_{[8:0]}$) is written into the device.
L	–	L-H	During the Data portion of a Write sequence, the single byte ($D_{[8:0]}$) is written into the device.
H	L-H	–	No data is written into the device during this portion of a Write operation.
H	–	L-H	No data is written into the device during this portion of a Write operation.

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction codes). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction

is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is given during the “Update IR” state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

EXTEST Output Bus Tri-State

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

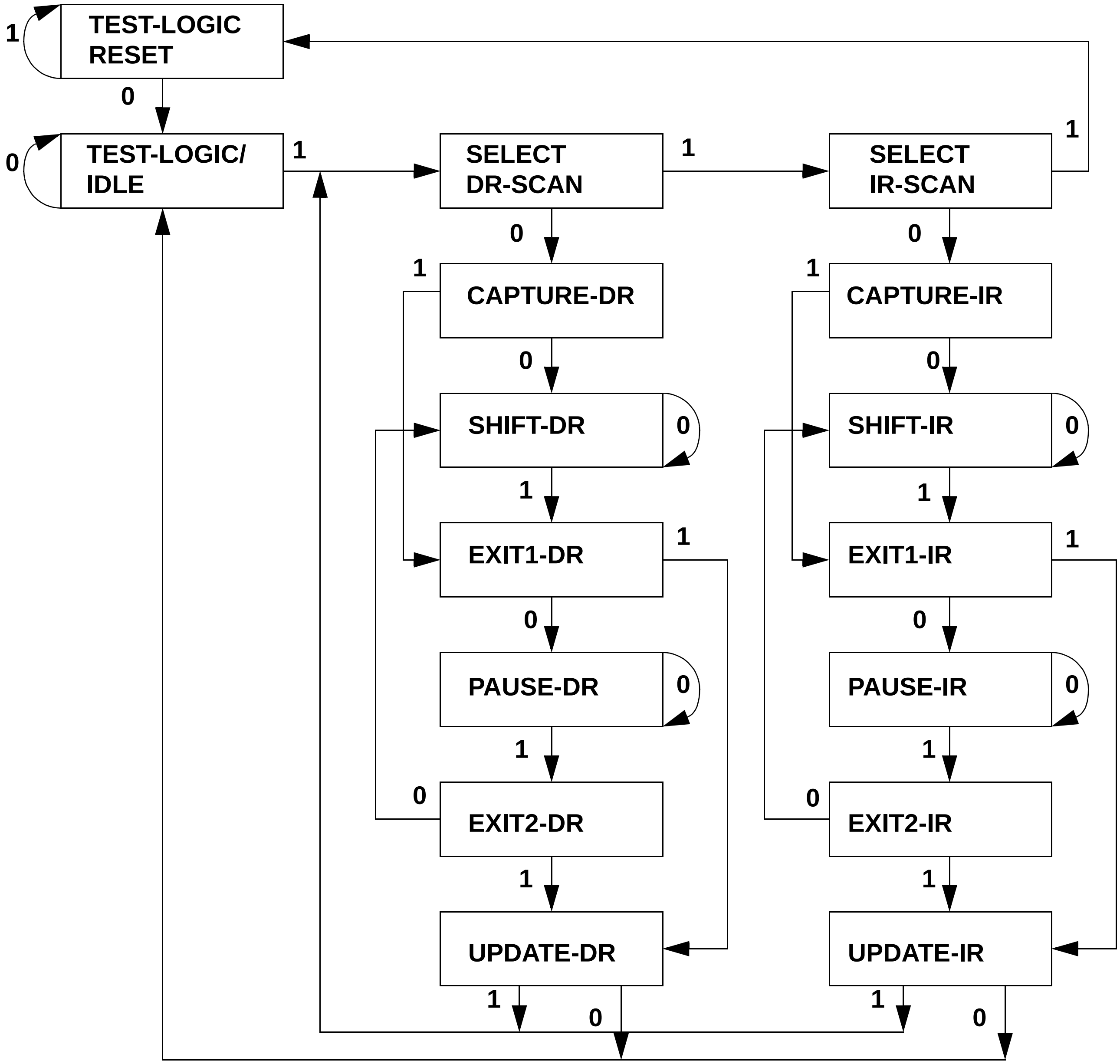
The boundary scan register has a special bit located at bit #47. When this scan cell, called the “extest output bus tri-state”, is latched into the preload register during the “Update-DR” state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the “Shift-DR” state. During “Update-DR”, the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the “Test-Logic-Reset” state.

Reserved

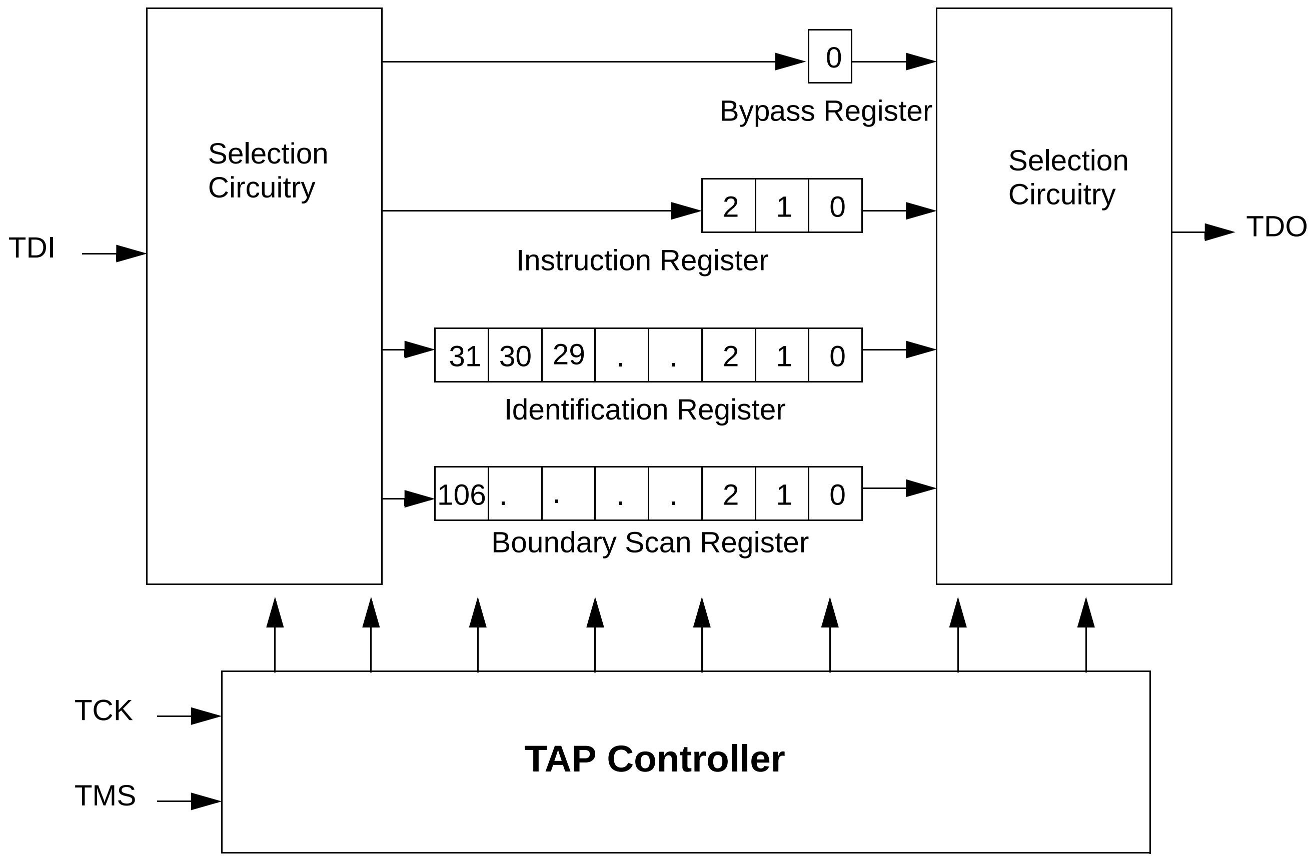
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram[9]



Note:
9. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[10, 13, 14]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	$I_{OH} = -2.0$ mA	1.4		V
V_{OH2}	Output HIGH Voltage	$I_{OH} = -100$ µA	1.6		V
V_{OL1}	Output LOW Voltage	$I_{OL} = 2.0$ mA		0.4	V
V_{OL2}	Output LOW Voltage	$I_{OL} = 100$ µA		0.2	V
V_{IH}	Input HIGH Voltage		$0.65V_{DD}$	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage		–0.3	$0.35V_{DD}$	V
I_X	Input and OutputLoad Current	$GND \le V_I \le V_{DD}$	–5	5	µA

TAP AC Switching Characteristics Over the Operating Range[11, 12]

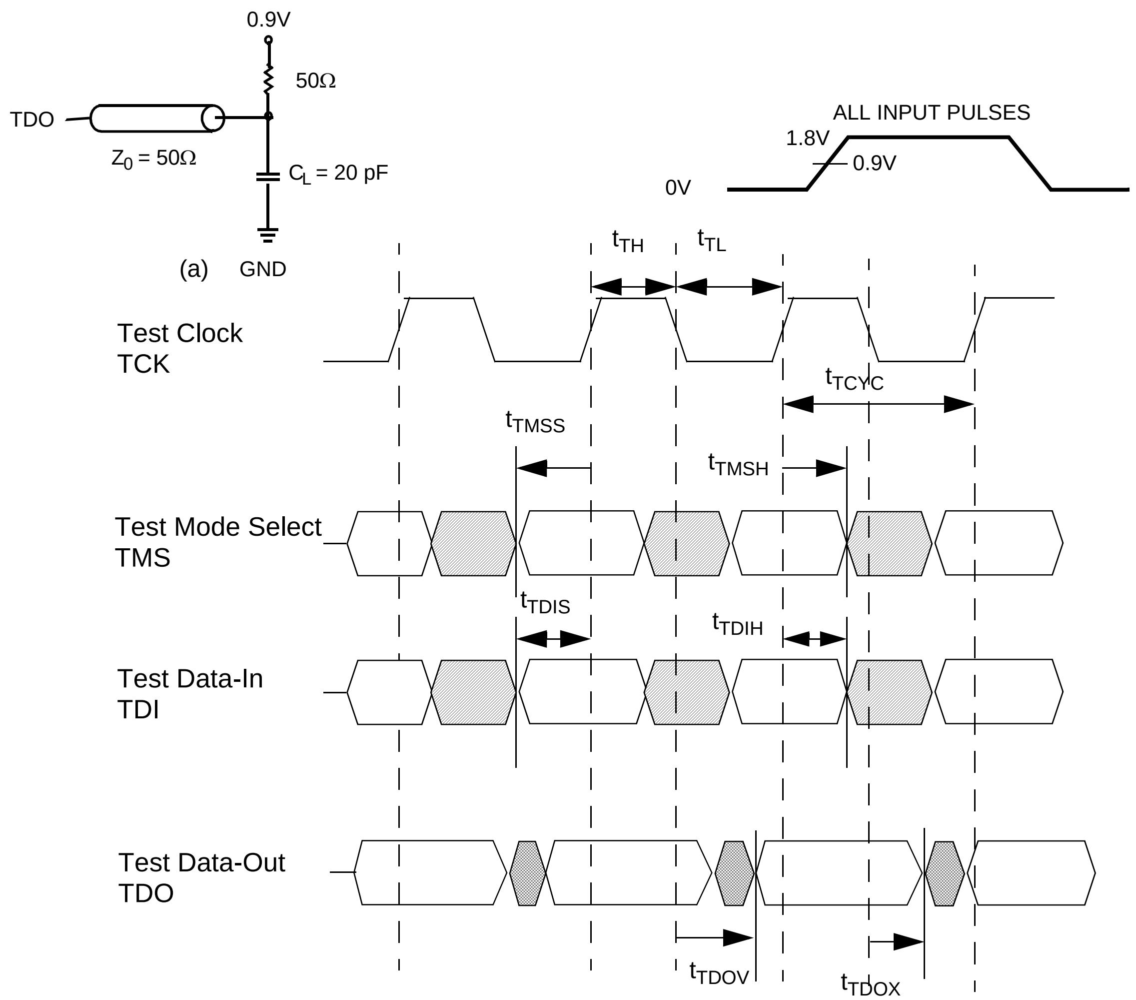
Parameter	Description	Min.	Max.	Unit
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH	20		ns
t_{TL}	TCK Clock LOW	20		ns

Notes:
10. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics Table.
11. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
12. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.
13. Overshoot: $V_{IH}(AC) \le V_{DD}$+0.85V (Pulse width less than $t_{TCYC}/2$); Undershoot $V_{IL}(AC) > -1.5V$ (Pulse width less than $t_{TCYC}/2$).
14. All voltage referenced to ground.

TAP AC Switching Characteristics Over the Operating Range[11, 12] (continued)

Parameter	Description	Min.	Max.	Unit
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	5		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	5		ns
t_{CS}	Capture Set-up to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

TAP Timing and Test Conditions[12]



Identification Register Definitions

Instruction Field	Value				Description
	CY7C1316CV18	CY7C1916CV18	CY7C1318CV18	CY7C1320CV18	
Revision Number (31:29)	001	001	001	001	Version number.
Cypress Device ID (28:12)	11010100010000101	11010100010001101	11010100010010101	11010100010100101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	1	1	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID
0	6R	28	10G	56	6A	84	2J
1	6P	29	9G	57	5B	85	3K
2	6N	30	11F	58	5A	86	3J
3	7P	31	11G	59	4A	87	2K
4	7N	32	9F	60	5C	88	1K
5	7R	33	10F	61	4B	89	2L
6	8R	34	11E	62	3A	90	3L
7	8P	35	10E	63	1H	91	1M
8	9R	36	10D	64	1A	92	1L
9	11P	37	9E	65	2B	93	3N
10	10P	38	10C	66	3B	94	3M
11	10N	39	11D	67	1C	95	1N
12	9P	40	9C	68	1B	96	2M
13	10M	41	9D	69	3D	97	3P
14	11N	42	11B	70	3C	98	2N
15	9M	43	11C	71	1D	99	2P
16	9N	44	9B	72	2C	100	1P
17	11L	45	10B	73	3E	101	3R
18	11M	46	11A	74	2D	102	4R
19	9L	47	Internal	75	2E	103	4P
20	10L	48	9A	76	1E	104	5P
21	11K	49	8B	77	2F	105	5N
22	10K	50	7C	78	3F	106	5R
23	9J	51	6C	79	1G		
24	9K	52	8A	80	1F		
25	10J	53	7A	81	3G		
26	11J	54	7B	82	2G		
27	11H	55	6B	83	1J		

Power-up Sequence in DDR-II SRAM[15]

DDR-II SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

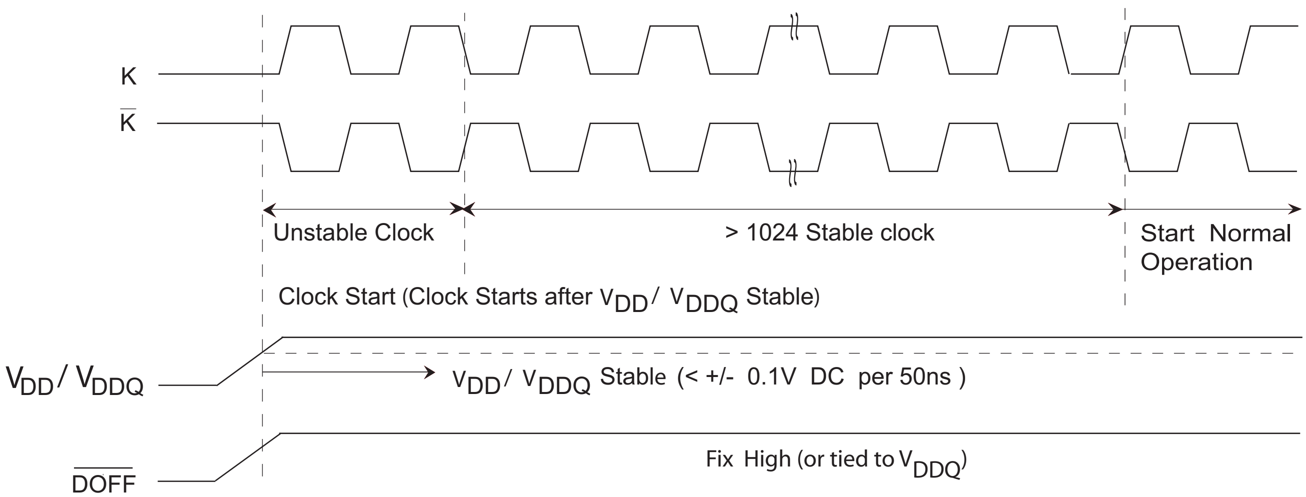
Power-up Sequence

- Apply power and drive $\overline{DOFF}$ LOW (All other inputs can be HIGH or LOW)
  — Apply V_{DD} before V_{DDQ}
  — Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}
- After the power and clock (K, $\overline{K}$) are stable take $\overline{DOFF}$ HIGH
- The additional 1024 cycles of clocks are required for the DLL to lock.

DLL Constraints

- DLL uses K clock as its synchronizing input. The input should have low phase jitter, which is specified as $t_{KC\ Var}$.
- The DLL will function at frequencies down to 80 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 1024 cycles stable clock to relock to the desired clock frequency

Power-up Waveforms



Note:
15. During Power-Up, when the DOFF is tied HIGH, the DLL gets locked after 1024 cycles of stable clock.

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with Power Applied ....–10°C to +85°C

Supply Voltage on V_{DD} Relative to GND........ –0.5V to +2.9V

Supply Voltage on V_{DDQ} Relative to GND ...... –0.5V to $+V_{DD}$

DC Applied to Outputs in High-Z......... –0.5V to V_{DDQ} + 0.3V

DC Input Voltage[13] ....–0.5V to V_{DD} + 0.3V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage (MIL-STD-883, M 3015).... >2001V

Latch-up Current.. >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}[16]	V_{DDQ}[16]
Com'l	0°C to +70°C	1.8 ± 0.1V	1.4V to V_{DD}
Ind'l	–40°C to +85°C		

Electrical Characteristics Over the Operating Range[14]

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage			1.7	1.8	1.9	V
V_{DDQ}	I/O Supply Voltage			1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH Voltage	Note 17		$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW Voltage	Note 18		$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH Voltage	I_{OH} = –0.1 mA, Nominal Impedance		V_{DDQ} – 0.2		V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW Voltage	I_{OL} = 0.1 mA, Nominal Impedance		V_{SS}		0.2	V
V_{IH}	Input HIGH Voltage			V_{REF} + 0.1		V_{DDQ} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3		V_{REF} – 0.1	V
I_X	Input Leakage Current	GND ≤ V_I ≤ V_{DDQ}		–5		5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5		5	µA
V_{REF}	Input Reference Voltage[19]	Typical Value = 0.75V		0.68	0.75	0.95	V
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	167 MHz			450	mA
			200 MHz			500	mA
			250 MHz			550	mA
			278 MHz			580	mA
			300 MHz			600	mA
I_{SB1}	Automatic Power-down Current	Max. V_{DD}, Both Ports Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$, Inputs Static	167 MHz			200	mA
			200 MHz			220	mA
			250 MHz			240	mA
			278 MHz			250	mA
			300 MHz			260	mA

AC Input Requirements Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage[13]		V_{REF} + 0.2	–	–	V
V_{IL}	Input LOW Voltage[13]		–	–	V_{REF} – 0.2	V

Capacitance[20]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5V	5	pF
C_{CLK}	Clock Input Capacitance		6	pF
C_O	Output Capacitance		7	pF

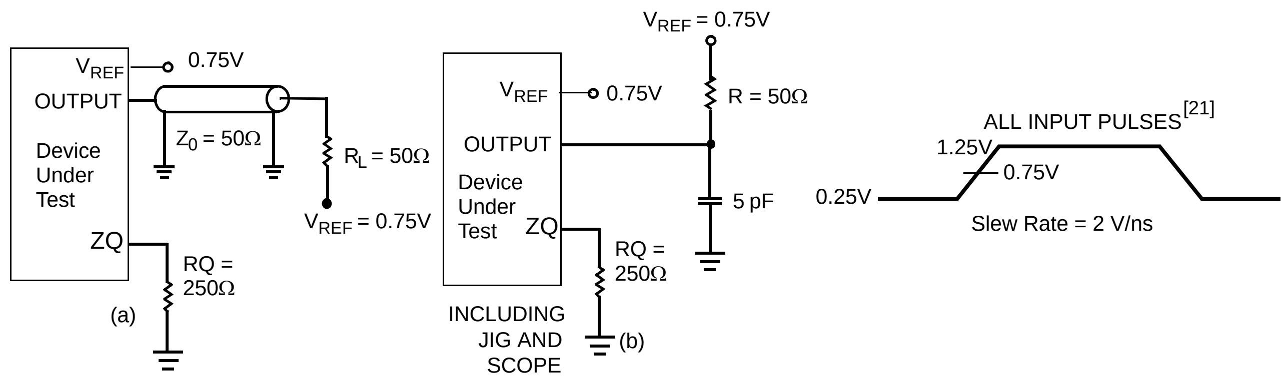
Notes:

16. Power-up: Assumes a linear ramp from 0V to V_{DD}(Min.) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
17. Outputs are impedance controlled. $I_{OH} = –(V_{DDQ}/2)/(RQ/5)$ for values of 175Ω ≤ RQ ≤ 350Ω.
18. Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175Ω ≤ RQ ≤ 350Ω.
19. V_{REF} (Min.) = 0.68V or 0.46V_{DDQ}, whichever is larger, V_{REF} (Max.) = 0.95V or 0.54V_{DDQ}, whichever is smaller.
20. Tested initially and after any design or process change that may affect these parameters.

Thermal Resistance[20]

Parameter	Description	Test Conditions	165 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	28.51	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		5.91	°C/W

AC Test Loads and Waveforms



Note:

21. Unless otherwise noted, test conditions assume signal transition time of 2V/ns, timing reference levels of 0.75V, V_{REF} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads.

Switching Characteristics Over the Operating Range [21, 22]

Cypress Parameter	Consortium Parameter	Description	300 MHz		278 MHz		250 MHz		200 MHz		167 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{POWER}		V_{DD}(Typical) to the first Access[23]	1	–	1	–	1		1		1		ms
t_{CYC}	t_{KHKH}	K Clock and C Clock Cycle Time	3.30	5.25	3.60	5.25	4.0	6.3	5.0	7.9	6.0	8.4	ns
t_{KH}	t_{KHKL}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH	1.32	–	1.4	–	1.6	–	2.0	–	2.4	–	ns
t_{KL}	t_{KLKH}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) LOW	1.32	–	1.4	–	1.6	–	2.0	–	2.4	–	ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K Clock Rise to $\overline{K}$ Clock Rise and C to $\overline{C}$ Rise (rising edge to rising edge)	1.49	–	1.6	–	1.8	–	2.2	–	2.7	–	ns
t_{KHCH}	t_{KHCH}	K/$\overline{K}$ Clock Rise to C/$\overline{C}$ Clock Rise (rising edge to rising edge)	0.00	1.45	0.00	1.55	0.0	1.8	0.0	2.2	0.0	2.7	ns
Set-up Times													
t_{SA}	t_{AVKH}	Address Set-up to K Clock Rise	0.4	–	0.4	–	0.5	–	0.6	–	0.7	–	ns
t_{SC}	t_{IVKH}	Control Set-up to Clock (K, $\overline{K}$) Rise ($\overline{LD}$, R/$\overline{W}$)	0.4	–	0.4	–	0.5	–	0.6	–	0.7	–	ns
t_{SCDDR}	t_{IVKH}	Double Data Rate Control Set-up to Clock (K, $\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.3	–	0.3	–	0.35	–	0.4	–	0.5	–	ns
t_{SD}[24]	t_{DVKH}	$D_{[X:0]}$ Set-up to Clock (K and $\overline{K}$) Rise	0.3	–	0.3	–	0.35	–	0.4	–	0.5	–	ns
Hold Times													
t_{HA}	t_{KHAX}	Address Hold after Clock (K and $\overline{K}$) Rise	0.4	–	0.4	–	0.5	–	0.6	–	0.7	–	ns
t_{HC}	t_{KHIX}	Control Hold after Clock (K and $\overline{K}$) Rise ($\overline{LD}$, R/$\overline{W}$)	0.4	–	0.4	–	0.5	–	0.6	–	0.7	–	ns
t_{HCDDR}	t_{KHIX}	Double Data Rate Control Hold after Clock (K and $\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.3	–	0.3	–	0.35	–	0.4	–	0.5	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ Hold after Clock (K and $\overline{K}$) Rise	0.3	–	0.3	–	0.35	–	0.4	–	0.5	–	ns
Output Times													
t_{CO}	t_{CHQV}	C/$\overline{C}$ Clock Rise (or K/$\overline{K}$ in single clock mode) to Data Valid	–	0.45	–	0.45	–	0.45	–	0.45	–	0.50	ns
t_{DOH}	t_{CHQX}	Data Output Hold after Output C/$\overline{C}$ Clock Rise (Active to Active)	–0.45	–	–0.45	–	–0.45	–	–0.45	–	–0.50	–	ns
t_{CCQO}	t_{CHCQV}	C/$\overline{C}$ Clock Rise to Echo Clock Valid	–	0.45	–	0.45	–	0.45	–	0.45	–	0.50	ns

Notes:

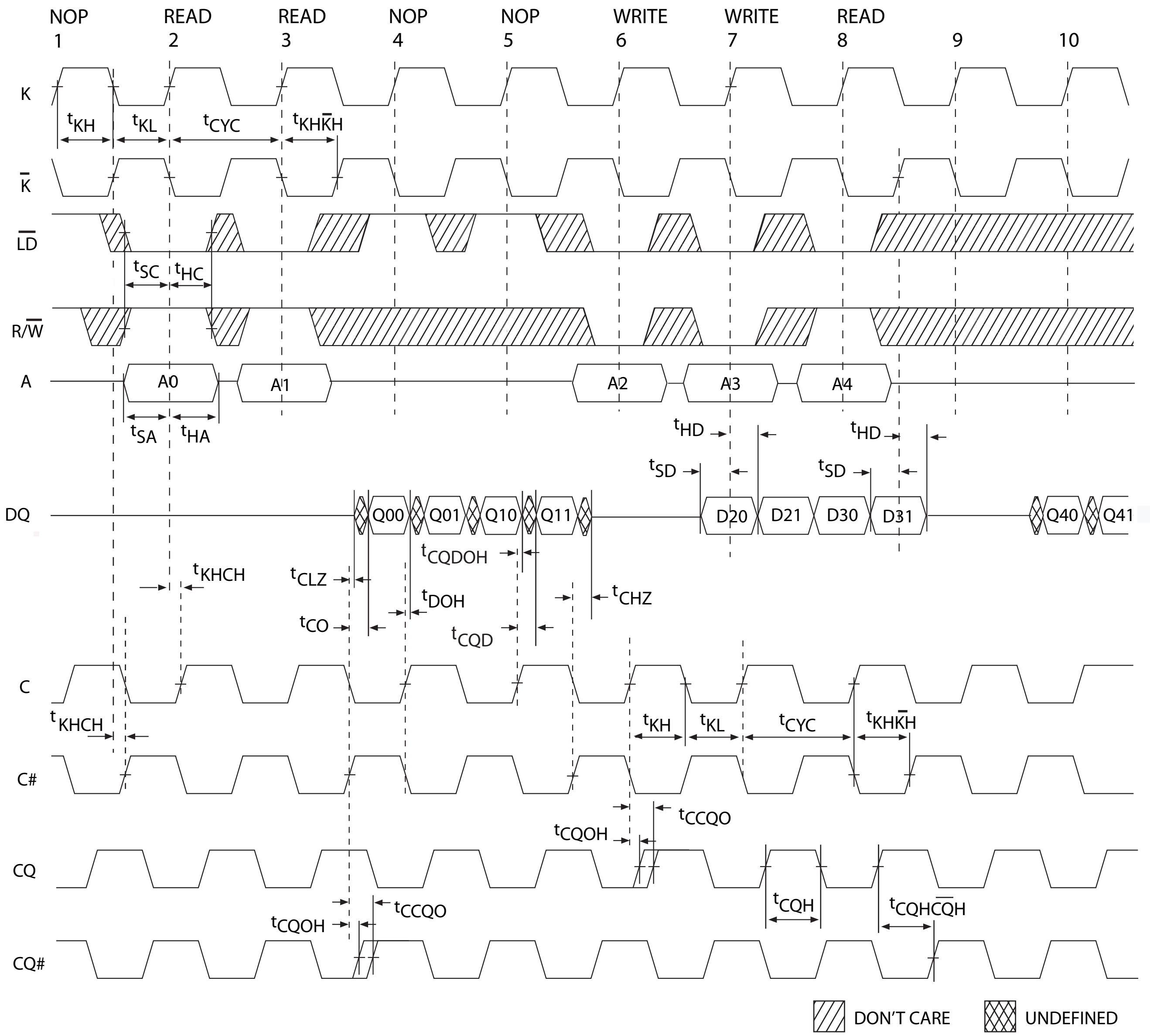
22. All devices can operate at clock frequencies as low as 119 MHz. When a part with a maximum frequency above 133 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and will output data with the output timings of that frequency range.
23. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
24. For DQ2 data signal on CY7C1916CV18 device, t_{SD} is 0.5ns for 200MHz, 250MHz, 278MHz and 300MHz frequencies.

Switching Characteristics Over the Operating Range (continued)[21, 22]

Cypress Parameter	Consortium Parameter	Description	300 MHz		278 MHz		250 MHz		200 MHz		167 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CQOH}	t_{CHCQX}	Echo Clock Hold after C/$\overline{C}$ Clock Rise	–0.45	–	–0.45	–	–0.45	–	–0.45	–	–0.50	–	ns
t_{CQD}	t_{CQHQV}	Echo Clock High to Data Valid	–	0.27	–	0.27	–	0.30	–	0.35	–	0.40	ns
t_{CQDOH}	t_{CQHQX}	Echo Clock High to Data Invalid	–0.27	–	–0.27	–	–0.30	–	–0.35	–	–0.40	–	ns
t_{CQH}	t_{CQHCQL}	Output Clock (CQ/$\overline{CQ}$) HIGH[25]	1.24	–	1.35	–	1.55	–	1.95	–	2.45	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ Clock Rise to $\overline{CQ}$ Clock Rise[25] (rising edge to rising edge)	1.24	–	1.35	–	1.55	–	1.95	–	2.45	–	ns
t_{CHZ}	t_{CHQZ}	Clock (C and $\overline{C}$) Rise to High-Z (Active to High-Z)[26, 27]	–	0.45	–	0.45	–	0.45	–	0.45	–	0.50	ns
t_{CLZ}	t_{CHQX1}	Clock (C and $\overline{C}$) Rise to Low-Z[26, 27]	–0.45	–	–0.45	–	–0.45	–	–0.45	–	–0.50	–	ns
DLL Timing													
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock Phase Jitter	–	0.20	–	0.20	–	0.20	–	0.20	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	DLL Lock Time (K, C)	1024	–	1024	–	1024	–	1024	–	1024	–	Cycles
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K Static to DLL Reset	30	–	30	–	30		30		30		ns

Notes:
25. These parameters are extrapolated from the input timing parameters ($t_{KH\overline{K}H}$ - 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps ($t_{KC\ Var}$) ia already included in the $t_{KH\overline{K}H}$). These parameters are only guaranteed by design and are not tested in production.
26. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 100 mV from steady-state voltage.
27. At any given voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.

Switching Waveforms[28, 29, 30]



Notes:
28. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, i.e., A0 + 1.
29. Outputs are disabled (High-Z) one clock cycle after a NOP.
30. In this example, if address A2 = A1,then data Q20 = D10 and Q21 = D11. Write data is forwarded immediately as read results. This note applies to the whole diagram.

Ordering Information

"Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered".

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
300	CY7C1316CV18-300BZC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1318CV18-300BZC			
	CY7C1320CV18-300BZC			
	CY7C1916CV18-300BZC			
300	CY7C1316CV18-300BZXC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Commercial
	CY7C1318CV18-300BZXC			
	CY7C1320CV18-300BZXC			
	CY7C1916CV18-300BZXC			
300	CY7C1316CV18-300BZI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1318CV18-300BZI			
	CY7C1320CV18-300BZI			
	CY7C1916CV18-300BZI			
300	CY7C1316CV18-300BZXI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Industrial
	CY7C1318CV18-300BZXI			
	CY7C1320CV18-300BZXI			
	CY7C1916CV18-300BZXI			
278	CY7C1316CV18-278BZC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1318CV18-278BZC			
	CY7C1320CV18-278BZC			
	CY7C1916CV18-278BZC			
278	CY7C1316CV18-278BZXC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Commercial
	CY7C1318CV18-278BZXC			
	CY7C1320CV18-278BZXC			
	CY7C1916CV18-278BZXC			
278	CY7C1316CV18-278BZI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1318CV18-278BZI			
	CY7C1320CV18-278BZI			
	CY7C1916CV18-278BZI			
278	CY7C1316CV18-278BZXI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Industrial
	CY7C1318CV18-278BZXI			
	CY7C1320CV18-278BZXI			
	CY7C1916CV18-278BZXI			
250	CY7C1316CV18-250BZC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1318CV18-250BZC			
	CY7C1320CV18-250BZC			
	CY7C1916CV18-250BZC			
250	CY7C1316CV18-250BZXC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Commercial
	CY7C1318CV18-250BZXC			
	CY7C1320CV18-250BZXC			
	CY7C1916CV18-250BZXC			

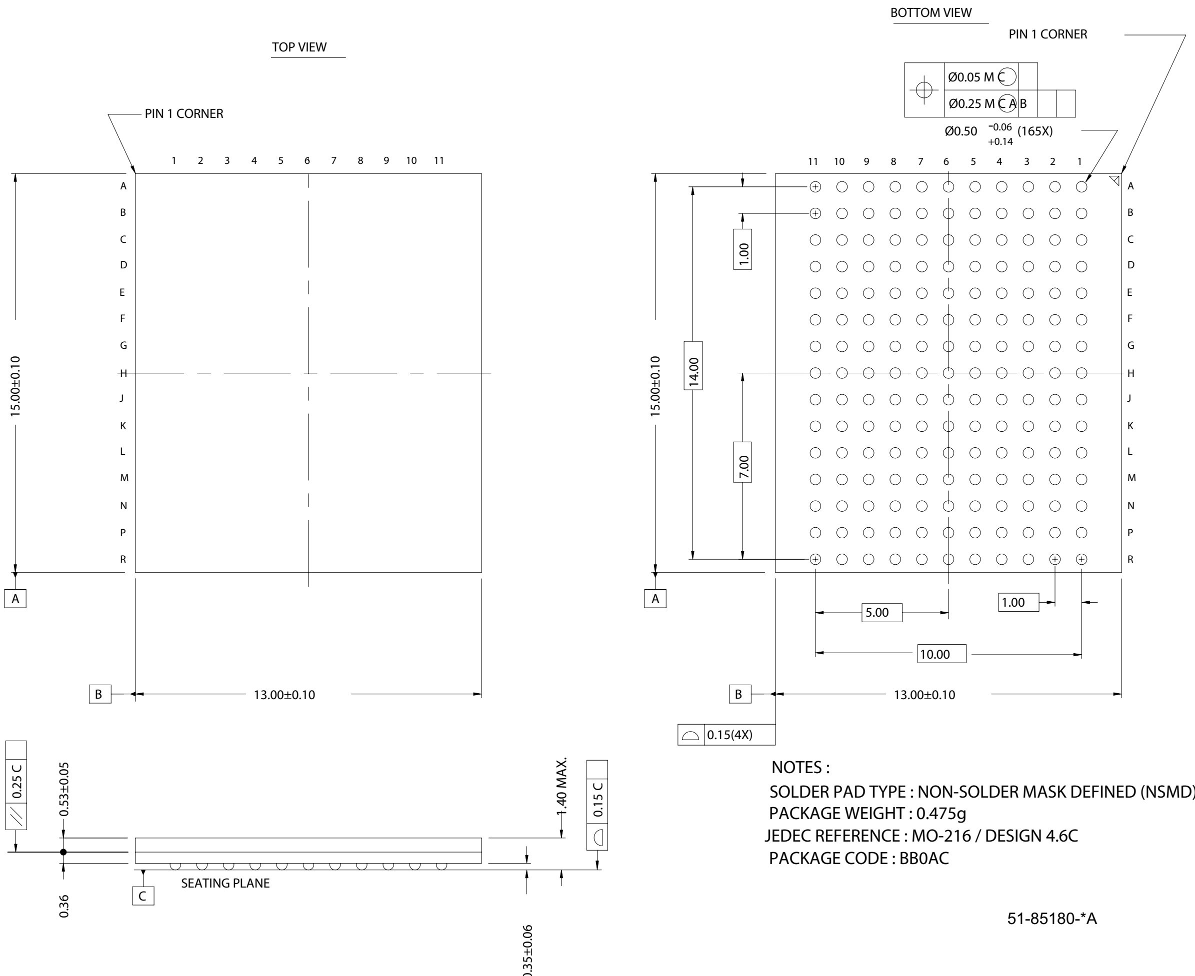
Ordering Information (continued)

"Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered".

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
250	CY7C1316CV18-250BZI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1318CV18-250BZI			
	CY7C1320CV18-250BZI			
	CY7C1916CV18-250BZI			
250	CY7C1316CV18-250BZXI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Industrial
	CY7C1318CV18-250BZXI			
	CY7C1320CV18-250BZXI			
	CY7C1916CV18-250BZXI			
200	CY7C1316CV18-200BZC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1318CV18-200BZC			
	CY7C1320CV18-200BZC			
	CY7C1916CV18-200BZC			
200	CY7C1316CV18-200BZXC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Commercial
	CY7C1318CV18-200BZXC			
	CY7C1320CV18-200BZXC			
	CY7C1916CV18-200BZXC			
200	CY7C1316CV18-200BZI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1318CV18-200BZI			
	CY7C1320CV18-200BZI			
	CY7C1916CV18-200BZI			
200	CY7C1316CV18-200BZXI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Industrial
	CY7C1318CV18-200BZXI			
	CY7C1320CV18-200BZXI			
	CY7C1916CV18-200BZXI			
167	CY7C1316CV18-167BZC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1318CV18-167BZC			
	CY7C1320CV18-167BZC			
	CY7C1916CV18-167BZC			
167	CY7C1316CV18-167BZXC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Commercial
	CY7C1318CV18-167BZXC			
	CY7C1320CV18-167BZXC			
	CY7C1916CV18-167BZXC			
167	CY7C1316CV18-167BZI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1318CV18-167BZI			
	CY7C1320CV18-167BZI			
	CY7C1916CV18-167BZI			
167	CY7C1316CV18-167BZXI	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	Industrial
	CY7C1318CV18-167BZXI			
	CY7C1320CV18-167BZXI			
	CY7C1916CV18-167BZXI			

Package Diagram

165-ball FBGA (13 x 15 x 1.4 mm) (51-85180)



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Document History Page

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REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	433284	See ECN	NXR	New data sheet
*A	462615	See ECN	NXR	Changed t_{TH} and t_{TL} from 40 ns to 20 ns, changed t_{TMSS}, t_{TDIS}, t_{CS}, t_{TMSH}, t_{TDIH}, t_{CH} from 10 ns to 5 ns and changed t_{TDOV} from 20 ns to 10 ns in TAP AC Switching Characteristics table Modified Power-Up waveform
*B	503690	See ECN	VKN	Minor change: Moved data sheet to web